REMARKS

In an Office Action mailed on March 24, 2005, claim 1 was rejected under 35 U.S.C. § 101 due to double patenting in view of claim 1 of prior U.S. Patent No. 6,615,331; claims 1, 37, 42, 43, 46, 52, 57, 58, 61, 65 and 67 were rejected under 35 U.S.C. § 112, first paragraph as failing to comply with a written description requirement; and claims 1 and 37-71 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Roy in view of Hsu. Claim 1 has been cancelled, and thus, the double patenting rejection has been overcome. The §§ 103 and 112 rejections are discussed below.

§ 112, First Paragraph Rejections:

Claims 1, 37, 42, 43, 46, 52, 57, 58, 61, 65 and 67 are rejected under 35 U.S.C. § 112, first paragraph as allegedly failing to comply with the written description requirement. However, the Examiner fails to establish a *prima facie* case by providing reasons why a person skilled in the art at the time the application was filed would not have recognized that the inventor was in possession of the invention as claimed. M.P.E.P. § 2163.04.I. More specifically, the Examiner merely concludes that the specification "fails to describe procedures on how to perform and carry out such process." Office Action, 3. This requirement, however, is not part of the written description requirement. In other words, as noted by the Examiner, the specification clearly references performing column redundancy checks, and thus, a skilled artisan would recognize that the inventor was in possession of the invention, due to these references alone to column redundancy checks.

It appears the Examiner may be implicitly rejecting the claims due to an alleged lack of enablement, which is a separate issue from the written description requirement. However, Applicant points out that, in general, circuitry to perform a "column redundancy check" was well known as of the filing date of the application, as evidenced by the cited application Hsu.

It is noted that a description as filed is presumed to be adequate to satisfy the written description requirement unless or until sufficient evidence or reasoning to the contrary has been presented by the Examiner to rebut the presumption. M.P.E.P. § 2163.04; *See In re Marzocchi*, 439 F.2d 220, 224, 169 U.S.P.Q. 367, 370 (CCPA 1971). Because the Examiner has not presented any evidence or reasoning relating to why the skilled artisan would have failed ot

recognize that the inventor was in possession of the invention in view of the disclosure of the application, withdrawal of the § 112, first paragraph rejection is requested.

§ 103 Rejections of Claims 37-42:

The method of independent claim 37 includes performing a column redundancy check and synchronizing the beginning of an internal write operation to a memory cell array of the memory device to a clock signal.

The Examiner fails to establish a *prima facie* case of obviousness for independent claim 37 for at least the reason that the hypothetical combination of Roy and Hsu fails to teach or suggest all claim limitations. For example, Roy generally describes a multichannel memory architecture that includes a boundary 1 that defines an interface between a memory device 20 and one or more master devices 10 and 15. *See, for example*, Fig. 1 of Roy and the corresponding text in lines 40-47 in column 9 of Roy. Thus, the language cited by the Examiner, i.e., the language found in lines 26-29 and 10-12 in column 12, relates to clock synchronization for data transfer across a boundary between memory devices, not the synchronization of the beginning of an internal write operation to a memory cell of a memory device. Thus, as the Examiner relies on Roy for the alleged teaching of the synchronizing of claim 37, a *prima facie* case of obviousness has not been established for this claim.

It is noted that Hsu fails to teach or suggest the missing claim limitations, i.e., the synchronizing of claim 37. More specifically, Hsu discloses a normal bit-line selector signal (called "YS") or a redundancy bit-line selector signal (called "YSR") that enable a read/write operation. Hsu, 3:14-17. However, as depicted in Fig. 6 of Hsu, the enablement of the read/write operation does not occur in connection with the beginning of an internal write operation.

Claims 38-42 are patentable for at least the reason that these claims depend from an allowable claim. Therefore, for at least the reasons that are set forth above, withdrawal of the § 103 rejections of claims 37-42 is requested.

Rejections of Claims 43-51:

The method of independent claim 43 includes providing column select signals that are indicative of a column address to a memory cell array of a memory device. The method includes performing a column redundancy check prior to the initiation of the providing of the column select signals.

The Examiner fails to establish a *prima facie* case of obviousness for independent claim 43 for at least the reason that the hypothetical combination of Roy and Hsu fails to teach or suggest all claim limitations. As conceded by the Examiner, Roy fails to teach performing a column redundancy check prior to the initiation of the providing of the column select signals. Thus, the Examiner relies on Hsu for this teaching.

However, Hsu fails to address when column select signals that are indicative of a column address are provided to a memory cell array of its memory device. As such, for at least this reason, Hsu fails to teach when the providing of the column select signals occur with respect to Hsu's disclosed column redundancy check. Therefore, for at least this reason, neither Roy nor Hsu teaches or suggests the act of performing of claim 43. The Examiner cites to language found in column 1 of Hsu. However, this language merely references a bit-line selector signal (called "YS") or a redundancy bit-line selector signal (called "YSR"). These signals are not column select signals that are indicative of a column address.

Claims 44-51 are patentable for at least the reason that these claims depend from an allowance claim. Therefore, for at least the reasons that are set forth above, withdrawal of the § 103 rejections of claims 43-51 is requested.

Rejections of Claims 52-57:

The memory device of independent claim 52 includes a memory cell array, a first circuit and a second circuit. The first circuit performs a column redundancy check in response to a decoded address, and the second circuit synchronizes an initiation of an internal write operation to the memory cell array with a clock signal.

See discussion of independent claim 37 above. In particular, the hypothetical combination of Roy and Hsu fails to teach or suggest all limitations of claim 52; and thus, for at least this reason, a *prima facie* case of obviousness has not been established for this claim.

More specifically, as pointed out above in the discussion of independent claim 37, Roy fails to teach a circuit to synchronize an initiation of an internal write operation to a memory cell array with a clock signal. Instead of such a teaching, the cited language from Roy discusses data transactions that occur outside of the memory device, not an internal write operation to a memory cell array of a memory device. Furthermore, Hsu fails to teach or suggest the missing claim limitations.

Claims 53-57 are patentable for at least the reason that these claims depend from an allowance claim. Therefore, for at least the reasons that are set forth above, withdrawal of the § 103 rejections of claims 52-57 is requested.

Rejections of Claims 58-64:

The memory device of independent claim 58 includes a memory cell array, an addressing circuit and a control circuit. The control circuit causes the addressing circuit to perform a column redundancy check during a delay to accommodate variations in the timing of a data strobe signal and begin providing column select signals to the memory cell array after performing the column redundancy check.

The Examiner fails to establish a *prima facie* case of obviousness for independent claim 58 for at least the reason that the hypothetical combination of Roy and Hsu fails to teach or suggest a control circuit that performs a column redundancy check during a delay to accommodate variations in the timing of the data strobe signal. More specifically, the Examiner refers to the language in lines 18-21 in column 35 of Roy that discloses the use of "CLKIN pulses (called "CLKIN" pulse) to allow a delay in the write data path sufficient to match properly with corresponding column select signals. However, the Examiner fails to establish why one skilled in the art, *without knowledge of the claimed invention*, would have modified Roy in view of Hsu to derive the claimed invention (*emphasis added*). In other words, the Examiner fails to show where the prior art contains the suggestion or motivation to modify Roy's memory system so that a column redundancy check is performed while one or more of the CLKIN pulses are occurring. Without such a suggestion or motivation, a *prima facie* case of obviousness has not been established for claim 58. M.P.E.P. § 2143.

Claims 59-64 are patentable for at least the reason that these claims depend from an allowable claim. Therefore, for at least the reasons that are set forth above, withdrawal of the § 103 rejections of claims 58-64 is requested.

Rejections of Claims 65-71:

The computer system of independent claim 65 includes a memory device that is coupled to a memory bus and is adapted to establish a predetermined window of time to capture data and perform a column redundancy check in response to the memory operation during the predetermined window of time.

See discussion of independent claim 58 above. In particular, the Examiner fails to establish a *prima facie* case of obviousness for independent claim 65 for at least the reason that the Examiner fails to show where the prior art contains the alleged suggestion or motivation to modify Roy in view of Hsu to derive the claimed invention. More specifically, the Examiner refers to the alleged necessity to hold data bytes within a data input unit 178 for a period of time before sending the data for synchronization of the I/O write operation with a column select signal 181. Office Action, 10. However, the Examiner fails to show why one skilled in the art, *without knowledge of the claimed invention*, would have modified Roy in view of Hsu to perform a column redundancy check during this holding time. Without such a suggestion or motivation, a *prima facie* case of obviousness has not been set forth for claim 65.

Claims 66-71 are patentable for at least the reason that these claims depend from an allowance claim. Therefore, for at least the reasons that are set forth above, withdrawal of the § 103 rejections of claims 65-71 is requested.

CONCLUSION

In view of the foregoing, withdrawal of the §§ 103 and 112 rejections and a favorable action in the form of a Notice of Allowance are requested. The Commissioner is authorized to charge any additional fees, or credit any overpayment to Deposit Account No. 20-1504 (MCT.0047C1US).

Respectfully submitted,

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